REMARKS

Reconsideration and reexamination of this application in light of the above-amendments and the following remarks is respectfully requested. Claims 1-20 are pending in this application. By way of this response, Claims 1, 9, and 14 have been amended. Basis for the amendments can be found throughout the specification, claims, and drawings as originally filed. No new matter has been added. Reconsideration of the rejections set forth in the outstanding Office Action is respectfully requested in view of the preceding amended claims and the following remarks.

I. Rejection Under 35 U.S.C. §102

Claims 1, 5-6, 9, 12, 14-15, 17, and 19-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kawabata. Claims 1-20 stand rejected under 35 U.S.C. §102(e) as being anticipated by Taniguchi. In light of the above amendments and the following remarks, Applicants respectfully traverse the rejection.

Kawabata does not teach or suggest a delay circuit that is coupled to a delay lock loop circuit, which is responsive to the amplitude a control signal from the delay lock loop circuit, to delay an input signal by a second period that is a function of

the control signal amplitude, as recited in Claims 1, 9, and 14. Rather, Kawabata teaches a delay lock loop ("DLL") that includes a shift register, which controls the delay times of delay lines based on phase compare detection signals output by a phase comparator. [See e.g., Kawabata, Col.5:17-20.] Hence, the delay of the delay lines is set using multiple inputs to a phase comparator, which feeds a shift register. Depending on the contents of the shift register, the delay lines are subsequently set to a certain delay. However, there is no teaching or suggestion that delays generated by one or more of the delay lines are a function of the amplitude of a control signal from the delay lock loop. The Applicants teach that a control signal produced by a delay lock loop circuit may be used to set the delay of a delay circuit. Specifically, the delay is a function of the control signal amplitude. This compares with a phase comparator with multiple inputs that sets a shift register as is taught by Kawabata. Thus, the delay lock loop circuit may be used as a reference to delay the delay circuit, and dependency on a duty cycle of an input signal may be eliminated.

Taniguchi, alone or in combination with Kawabata, does not teach or suggest a delay circuit that is coupled to a delay lock loop circuit, which is responsive to the amplitude of a control signal from the delay lock loop circuit, to delay an input signal by a second period that is a function of the control

signal amplitude, as recited in Claims 1, 9, and 14. Taniguchi teaches that a phase comparing section is used to generate a phase error signal, which is then fed to delay control circuits. [See e.g., Taniguchi, Col.1:39-46.] Taniguchi fails to disclose that one delay control circuit may be responsive to the amplitude of a control signal from another delay circuit. As explained above, the Applicants disclose that the delay circuit is responsive to a control signal amplitude from the delay lock loop circuit to delay the period on an input signal.

Thus as presently claimed, Applicants respectfully submit that Claims 1-20 are not anticipated by Kawabata and Taniguchi either singly or in combination. Accordingly, Applicants respectfully request reconsideration and withdrawal of this rejection of Claims 1-20.

II. Conclusion

Applicants have carefully reviewed each of the objections and rejections set forth, and have amended the claims as indicated herein to individually address the rejections and objections and to place all claims in condition for allowance. In view of the above, Applicants submit that the specification and drawings are in order and that all the claims are now in condition for allowance. Such action is respectfully requested. Please apply any other charges or credits to Deposit Account

No. 06-1050. If the Examiner would like to discuss the matter further, the undersigned may be contacted at (858) 678-5070. Attached is a marked-up version of the changes being made by the current amendment.

Respectfully submitted,

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Joseph L. Stevenson
Reg. No. 43,163

Fish & Richardson P.C.
PTO Customer No. 20985
4350 La Jolla Village Drive, Suite 500
San Diego, California 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Claims 1, 9, and 14 have been amended as follows:

1. (Amended) A device, comprising:

a delay lock loop circuit responsive to an input signal to delay the input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to the input signal, the delay circuit being responsive to [a] the analog control signal from the delay lock loop circuit to delay the input signal by a second period as a function of the analog control signal amplitude.

9. (Amended) A device, comprising:

a delay lock loop circuit responsive to a first input signal to delay the first input signal by a first period and to generate an analog control signal having an amplitude; and

a delay circuit coupled to the delay lock loop circuit and responsive to a second input signal, the delay circuit being responsive to [a] the analog control signal from the delay lock

loop circuit to delay the second signal by a second period as a function of the analog control signal amplitude.

14. (Amended) A method, comprising:

receiving a first signal and a second signal;

using a delay lock loop circuit to delay the first signal by a first period;

controlling the first period as a function of an analog control signal having an amplitude; and

using a delay circuit to delay the second signal by a second period in response to [a] the analog control signal amplitude from the delay lock loop circuit.